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10/808,908	03/25/2004	David Walker Guidry	TI-37090	7410

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EXAMINER	
JEANGLAUDE, JEAN BRUNER	
ART UNIT	PAPER NUMBER
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,908	GUIDRY, DAVID WALKER	
	Examiner	Art Unit	
	Jean B. Jeanglaude	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-18 and 20-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-11,13-18 and 20-24* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response To Amendments/Arguments

Applicant's arguments with respect to claims 2 – 18, 20 - 24 have been considered but are moot in view of the new ground(s) of rejection.

The Prosecution on this case is reopened.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 18, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watson et al. US Patent Number 6,195,032) in view of Sevenhans et al. (US Patent Number 5,422,889) and Al-Awadhi . (US patent Number 6,683,550).

3. Regarding claims 18 and 24 Watson et al. discloses a successive approximation apparatus and method (fig 3) comprising a memory (latches) (42, 44, 46) having a successive approximation value (col. 5, lines 32 – 40); a summer (28) coupled to a test signal and output of the memory to generate a difference signal being a difference there between (fig. 3)[the difference is obtained before amplifying the signal); an amplifier (22) coupled to an output of the summer (28) to generate an amplified signal from the difference signal (fig. 3) and a multi-bit ADC (24) coupled to an output of the amplifier (22) to convert the amplified signal to a digital signal (fig. 3) wherein the analog to digital converter (24) operates as a comparator until the amplified

signal is within range of the ADC. Watson et al. does not explicitly disclose a SAR ADC that comprises a single multi-bit ADC coupled to an output of amplifier. However, Sevenhans et al. discloses a system (fig. 1) that comprises an ADC (note the single ADC in fig. 2) that is coupled to an output of an amplifier (A2) that converts the amplified signal (see col. 5, lines 55 – 63). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Watson et al.'s system with that of Sevenhans et al. in order to remove offset from an input signal being input thereto is assigned slots.

4. Moreover, the both Watson et al. and Sevenhans et al disclose all the limitations as discussed above except the system that has a multi-bit DAC. However, as noted in Al-Awadhi (fig. 1), a multi-bit ADC is used as a successive approximation analog to digital converter (abstract). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Watson et al. and Sevenhans et al.'s system with that of Al-Awadhi in order to convert an analog input signal into digital signal using multi-bit delta sigma modulator. The combination of the Watson et al., Sevenhans et al. and Al-Awadhi would achieve the same end result as the claimed invention.

5. Claims 2 – 11, 13 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watson et al. US Patent Number 6,195,032) in view Sevenhans et al. (US patent Number 5,422,889) and Al-Awadhi (US patent Number 6,683,550) as applied to claim 24 above, and further in view of Burns (US patent Number 5,589,763).

6. Regarding claim 2 – 11, 13 – 23, Watson et al. in combination with Sevenhans et al. and Al-Awadhi disclose all the limitations as discussed above except the successive approximation system further comprising logic operative to adjust the successive approximation value based on the digital signal (claim 3); a successive approximation system further comprising a clock source to produce clock signals, a signal generating circuit to generate and output a repetitive test waveform to a device under test in accordance with the clock signals, the device under test outputting the test signal and a pulse generating circuit coupled to the clock circuit for producing sampling point signals corresponding to sampling points spaced across the test signal based on the clock signals, a successive approximation system a comparison system further comprising a multi-bit analog to digital converter for converting the amplified signal to the digital signal, the multi-bit analog to digital converter having a range, the logic being responsive to adjust the successive approximation value based on the digital signal to place the digital signal within the range of the multi-bit analog to digital converter (claims 3, 9); a successive approximation system and method wherein the logic appends the digital signal to the successive approximation value to increase the resolution of the successive approximation value after the digital signal is within the range of the multi-bit analog to digital converter (claims 4, 21); a successive approximation system and method wherein the logic calibrates the digital signal in accordance with the successive approximation value after the digital signal is within the range of the multi-bit analog to digital converter (claims 5, 22); a successive approximation system and method the logic being operative to adjust the successive approximation value based on the digital

signal by performing a single bit iteration when the amplified signal is outside the range of the multi-bit analog to digital converter, starting with most significant bit first to least significant bit, until the amplified signal is within the range of the multi-bit analog to digital converter (claim 6, 20); a successive approximation system, the logic being operative to append a value of the digital signal to the least significant bits of the successive approximation value after the amplified signal is within range of the multi- bit analog to digital converter (claim 7); a successive approximation system and method the logic calibrating the digital signal according to the successive approximation value (claims 8, 23); a successive approximation system wherein the sampling point signals sample the test signal at a sample rate less than the Nyquist rate of the test signal (claim 10); a successive approximation system further comprising a second clock source producing a second clock signal, the pulse generating circuit being operative to determine a frequency ratio between the clock source and the second clock source and to employ the frequency ratio for producing the sampling point signals (claim 11); a successive approximation system wherein at least one of the pulse generating circuit memory, clock circuit, and signal generating circuit are implemented on the same integrated circuit as the circuit under test and the comparison system (claim 13); a coherent undersampling digitizer comprising: means for receiving a repetitive test signal from a device under test in accordance with first clock signals, means (the compare result) for producing a difference signal based on the difference between the repetitive test signal and a successive approximation signal means for amplifying the difference signal, and means for converting the amplified difference signal to a multi-bit digital

comparison signal (claim 14); a coherent undersampling digitizer (fig. 5), the means for converting producing a first signal when the amplified difference signal is outside a range of the means for converting, and producing a second signal indicative of magnitude of the amplified difference signal when the amplified difference signal is within the range of the means for converting (claim 15); a coherent undersampling digitizer, the means for producing sampling point signals being responsive to a ratio between the first clock signals and second clock signals and to generate the successive approximation signal based on the multi-bit digital comparison signal (claim 16); a coherent undersampling digitizer the means for producing sampling point signals generating single bit iterations of the successive approximation signal while the first signal is produced and a multi-bit iteration of the successive approximation signal when the second signal is produced (claim 17).

7. However, as per claims 3, 9, Burns discloses a successive approximation system (fig. 5), further comprising a clock source (208, fig. 5) to produce clock signals, a signal generating circuit (200, fig. 5) to generate and output a repetitive test waveform to a device under test in accordance with the clock signals, the device under test outputting the test signal (note test signal), and a pulse generating circuit (212) coupled to the clock circuit for producing sampling point signals corresponding to sampling points spaced across the test signal based on the clock signals (fig. 5). Also, it is noted in Burns that the input signal (200) may be either an analog or digital signal. In applying a digital signal as the input of Burns circuit an artisan in the art would recognize that an ADC will provide the digital signal to Burns' circuit and Burns' circuit comprises a

comparator (206) and logic circuit (218) and Watson, in related field, discloses an Analog/digital converter (fig. 4) that comprises a comparator (32, fig. 4) which includes a differential amplifier 42 which compares the input signals (37) and the output of a second DAC 35. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Watson et al. in combination with Sevenhans et al. and Al-Awadhi's system with that Burns' system in order to measure a repetitive signal in a coherent manner and the combination of Burns, Watson et al., Sevenhans et al. and Al-Awadhi's systems would achieve the same end result as the claim invention.

8. Regarding claims 4, and 21 Burns discloses a successive approximation system and method (fig. 5) wherein the logic (218) appends the digital signal to the successive approximation value to increase the resolution of the successive approximation value after the digital signal is within the range of the multi-bit analog to digital converter [it is inherent that the SAR would increase the resolution of the system] (fig. 5).

9. Regarding claims 5, 22, Burns discloses a successive approximation system and method (fig. 5) wherein the logic (218) calibrates the digital signal in accordance with the successive approximation value after the digital signal is within the range of the multi-bit analog to digital converter [it is inherent that the logic would calibrate the digital signal].

10. Regarding claims 6, and 20, Burns discloses a successive approximation system and method (figs. 5, 6), the logic (218) being operative to adjust the successive approximation value based on the digital signal by performing a single bit iteration when

the amplified signal is outside the range of the multi-bit analog to digital converter, starting with most significant bit first to least significant bit, until the amplified signal is within the range of the multi-bit analog to digital converter (figs. 5, 6).

11. Regarding claim 7, Burns discloses a successive approximation system (fig. 5), the logic (218) being operative to append a value of the digital signal to the least significant bits of the successive approximation value after the amplified signal is within range of the multi- bit analog to digital converter (figs. 5, 6).

12. Regarding claims 8, 23, Burns discloses a successive approximation system and method (fig. 5) the logic (218) calibrating the digital signal according to the successive approximation value (fig. 5)[it is inherent that the logic circuit would calibrate according to the SAR value].

13. Regarding claim 10, Burn discloses a successive approximation system (fig. 5) wherein the sampling point signals sample the test signal at a sample rate less than the Nyquist rate of the test signal (fig. 5).

14. Regarding claim 11, Burns discloses a successive approximation system (fig. 5), further comprising a second clock source (210) producing a second clock signal, the pulse generating circuit (212)[col 5, lines 31 – 34] being operative to determine a frequency ratio between the clock source and the second clock source and to employ the frequency ratio for producing the sampling point signals (fig. 5).

15. Regarding claim 13, Burns discloses a successive approximation system (fig. 5) wherein at least one of the pulse generating circuit (212), memory (218), clock circuit

(209), and signal generating circuit (200) are implemented on the same integrated circuit as the circuit under test (202) and the comparison system (206).

16. Regarding claim 14, Burns discloses a coherent undersampling digitizer (fig. 5), comprising: means (204) for receiving a repetitive test signal from a device under test (202) in accordance with first clock signals, means (the compare result) for producing a difference signal based on the difference between the repetitive test signal and a successive approximation signal means (216) for amplifying the difference signal, and means (220) for converting the amplified difference signal to a multi-bit digital comparison signal (fig. 5).

17. Regarding claim 15, Burns discloses a coherent undersampling digitizer (fig. 5), the means for converting producing a first signal when the amplified difference signal is outside a range of the means for converting, and producing a second signal indicative of magnitude of the amplified difference signal when the amplified difference signal is within the range of the means for converting (fig. 5).

18. Regarding claim 16, Burns discloses a coherent undersampling digitizer (fig. 5, the means (212) for producing sampling point signals being responsive to a ratio between the first clock signals and second clock signals and to generate the successive approximation signal based on the multi-bit digital comparison signal (fig. 5).

19. Regarding claim 17, Burns discloses a coherent undersampling digitizer (fig. 5) the means (212) for producing sampling point signals generating single bit iterations of the successive approximation signal while the first signal is produced and a multi-bit

iteration of the successive approximation signal when the second signal is produced (fig. 5).

20. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Watson et al.'s system with that of Burn in order to measure a repetitive signal in a coherent manner including a signal generating circuit to output the repetitive signal to a RUT in accordance with clock signals.

Allowable Subject Matter

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (See PTO-892).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jean Bruner Jeanglaude
Primary Examiner
September 13, 2006